SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SMART POWER PROCESSES FOR LSI CIRCUITS

by Carlo Cini

Over the years smart power technology has advanced to ever-increasing power and voltage levels. At the same time, almost unnoticed there has been a remarkable increase in the smartness of circuits -- the amount of complexity that can be integrated practically on one chip.

Today it is possible to integrate circuits like the one shown in figure 1, which contains two 1A motor drives, a 3A solenoid driver, a 1A switchmode power supply and a micro interface (this chip will be described in more detail later). Clearly the possibility of integrating so much of a system has a dramatic effect on the way system engineers approach partitioning; complexity is no longer limited by technology, but by economic factors.

The technologies that allow such circuits to be made are generally known as "BCD" technologies because they combine bipolar, CMOS and DMOS process structures. First introduced by SGS in 1986, they allow IC designers to use bipolar components when high precision is needed (in references etc), CMOS for high density digital and analog, and power DMOS for low dissipation output stages.

Low dissipation is, in fact, one of the key advantages of BCD technology. A DMOS power transistor in switchmode operation dissipates very little power so it is possible to deliver high power to the load without expensive power packaging and cooling systems (the power that can be dissipated inside an IC is determined by the package). Equally important is the fact that low dissipation power stages make it feasible to place several power stages on the same chip. This, together with the high density CMOS, makes high complexity circuits feasible.

BCD TECHNOLOGY

The first commercial process to combine bipolar, CMOS and power DMOS was the Multipower-BCD process introduced by SGS-THOMSON in 1986. A 60V technology, this was created by merging vertical DMOS technology with a conventional junction-isolated bipolar IC process (figure 2).

Figure 1: A High Complexity Smart Power IC Containing Multiple Drivers.

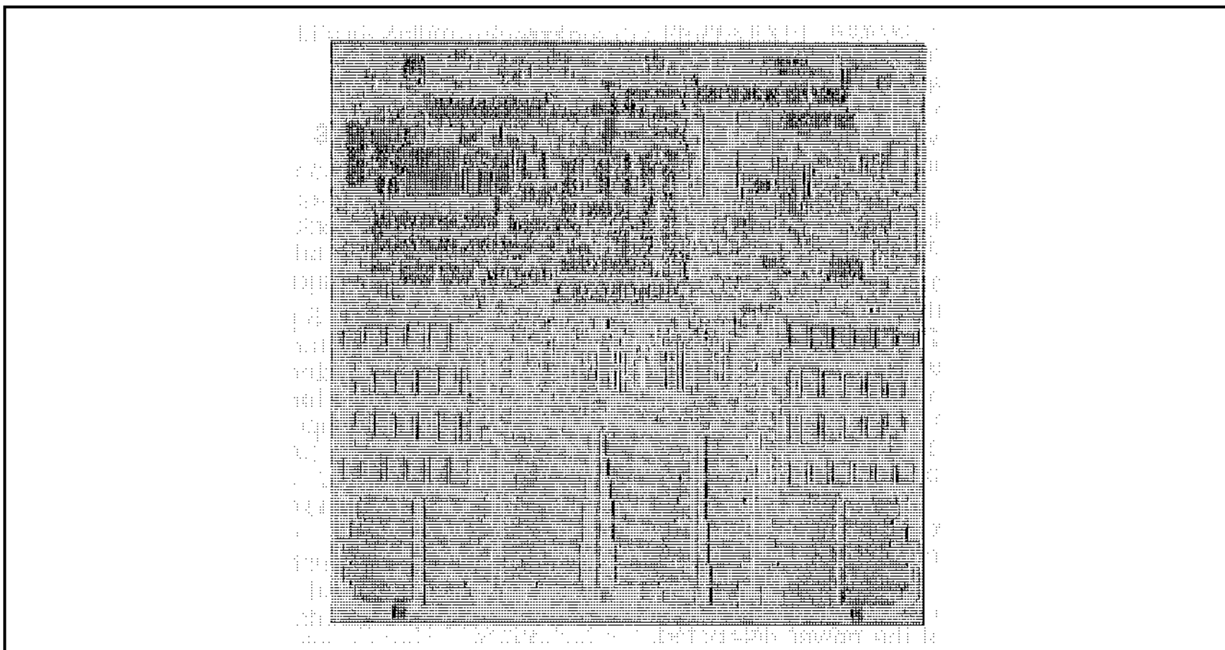
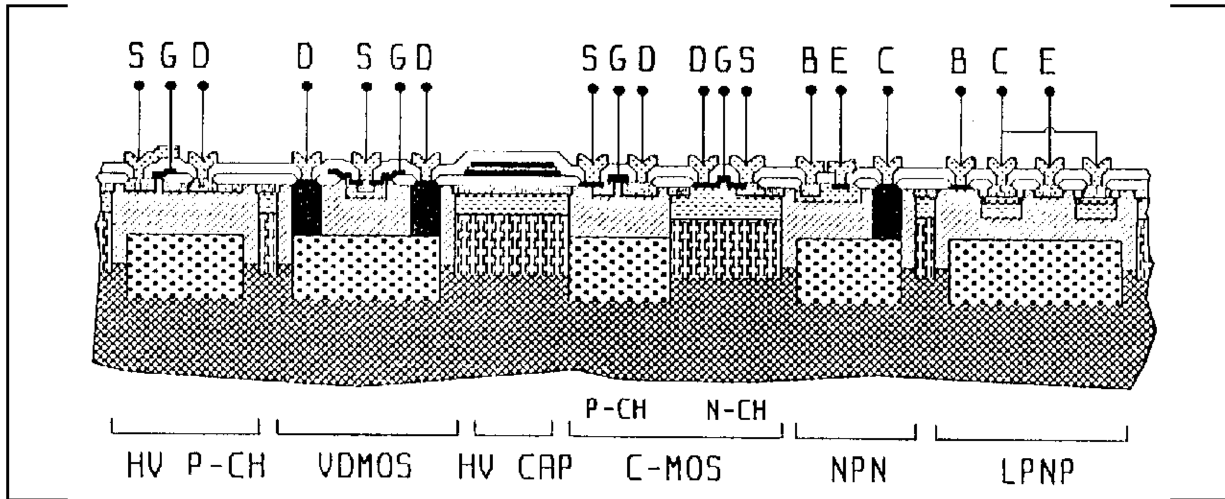


Figure 2: Cross Section of the Multipower-BCD Process.



An important characteristic of this technology is that it provided all of the contacts on the top surface of the die and completely isolated the power DMOS transistors. This was important because it allowed the integration of any kind of power stage: high side, low side, half bridge or bridge. Moreover, multiple power stages could be integrated on one chip.

Having bipolar, CMOS and DMOS structures available gives the designer freedom to choose the most appropriate for each part of the circuit. Bipolar structures are used primarily in linear functions where high precision is needed: low offsets, low drift and so on; it can also be useful in predriving stages. CMOS is useful both for high density logic and high density analog circuits where high precision is not needed.

DMOS power stages have several important advantages over their bipolar equivalents. Most important is the low dissipation, which is because DMOS devices need no driving current in DC conditions and operate very efficiently in high-speed switching applications. Other advantages include the freedom from second breakdown and the presence of an intrinsic freewheeling diode, which is useful with inductive loads.

Since the original 60V process was introduced several other process variations have been introduced: a 100V version, a 250V version and a new family of shrink processes called BCD-II, which use a 2.5u geometry. The evolution of these can be continuous and to give an idea of the improvement made and forecasted there are two values (Ron x area and number of transistors per square millimieter, which express clearly the strength of a technology. For the power components there is the Ron x Area parameter which indicates for a given area the reduction in ON resistance, and hence the improvement in the electrical efficiency, or rather, the reduction of the power dissipated. This parameter appears to improve by a factor of two every four years. In the signal section the most common parameter is the number of transistors per square millimeter. Here progress is more marked than in the power section because it is possible to exploit the knowhow existing in VLSI technology where the microlithography is the dominating factor and not the current.

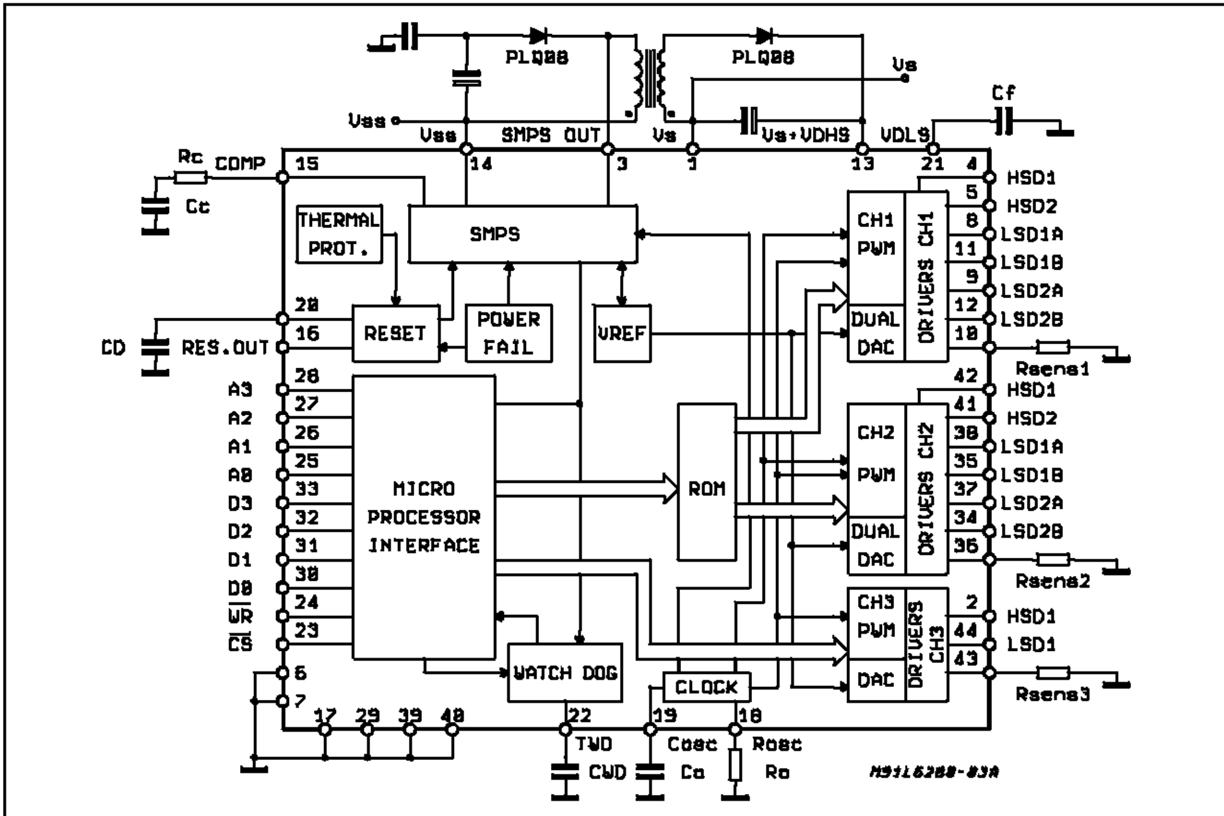
A high voltage (>600V) version is also close to introduction. The 60V and 100V versions cover the majority of applications today, in industrial, computer peripheral, automotive and consumer products. At present the main applications for 250V technology are in lamp ballasts and power supplies, though it is expected that when new high pressure gas discharge lamps are adopted by the automotive industry circuits in this technology will be appropriate. The expected uses of 500V technology are mainly in offline power supplies and home automation.

EXAMPLE PRODUCTS

We will now examine some typical BCD IC exemplify the remarkable versatility of the technology. Figure 3 shows the block diagram of a chip introduced in 1988 for a portable typewriter application -- the chip shown in figure 1.

This circuit integrates 15 power DMOS transistors and about 4000 other transistors. On this chip are all of the power subsystems needed in the typewriter: a 1A motor drive for the carriage positioner, a 1A motor drive for paper feed, a 1A motor drive for the daisy wheel, a 3A solenoid driver for the hammer and a 1A/5V switchmode supply that power the micro. In addition the chip includes all of the interface circuits, control logic and protection circuits. One interesting characteristic of this circuit is that most of the functions are programmed by loading internal registers. It is even possible to program output stage configurations,

Figure 3: Block Diagram of the Chip Shown in Figure 1.



an interesting concept that makes the device more flexible than one would expect from such a complex and highly-specific solution.

With the introduction of the shrink version, BCD-II, circuits of this complexity have become smaller and less expensive. Figure 4 shows a recent example of a custom circuit in BCD-II technology for a computer peripheral application that includes a servo positioning system, motor controller and various other functions that were not integrated on other ICs on the board.

Figure 4: Complex Smart Power Chip Realized with Shrunk BCD-II Process.

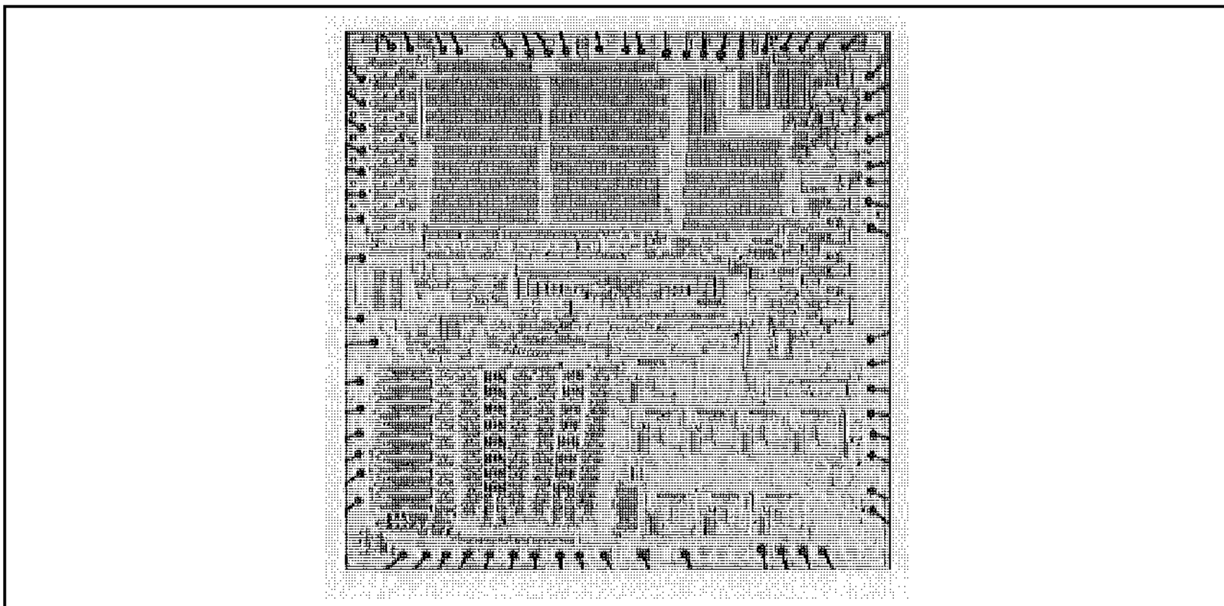
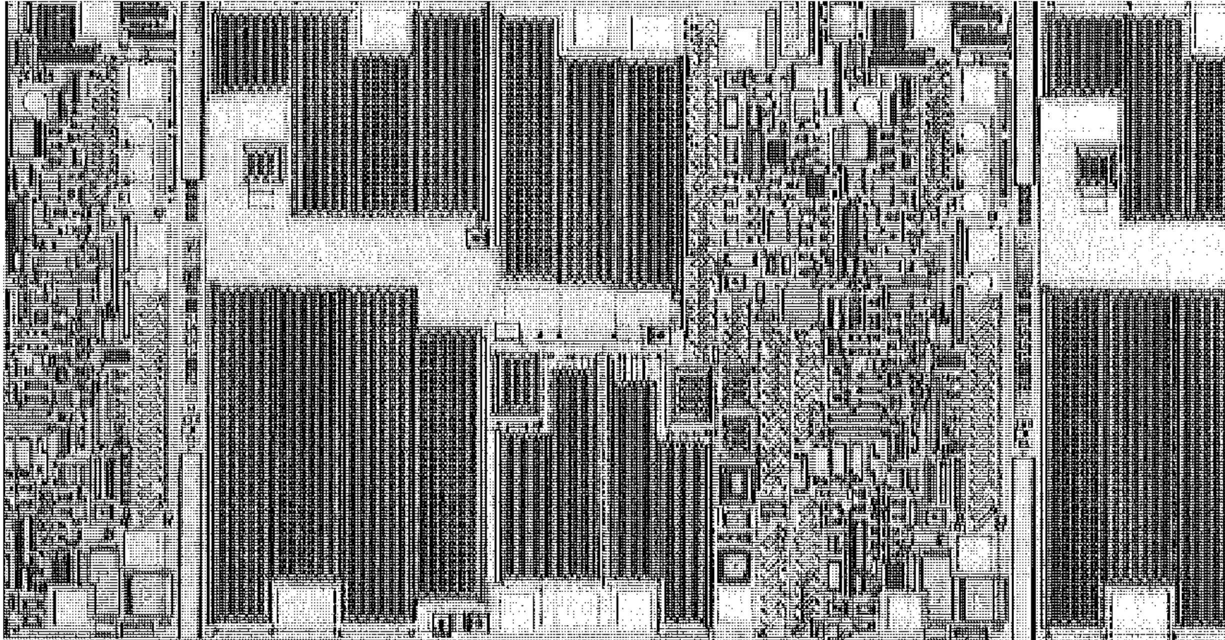


Figure 5: A Multiple Linear Regulator Chip in BCD Technology.



Though most BCD circuits use switchmode DMOS power stages it is also possible to use the technology in linear applications, as illustrated in figure 5, which shows a quad linear regulator chip. Designed for a car radio, this circuit contains four regulators (10V/60mA, 8V/50mA, 5V/300mA, 5V/600mA) with bipolar PNP pass transistors. BCD technology was chosen in this case for several reasons: low current drain, compact die size and the possibility of having an uninterrupted positive output even in the presence of a negative dump transient.

The circuit shown in figure 6 is an example of a multiple power chip for the automotive market. This chip is used in rearview mirror units and drives the three motors (mirror adjust up/down, adjust left/right and fold) plus the defroster heating element. Mixed bonding is employed in this circuit.

Figure 7 shows a practical high voltage IC fabricated in BCD250 technology for a compact fluorescent lamp ballast application. A DMOS bridge output stage is clearly visible.

Figure 6: Multiple Smart Power Chip for Car Mirror Control.

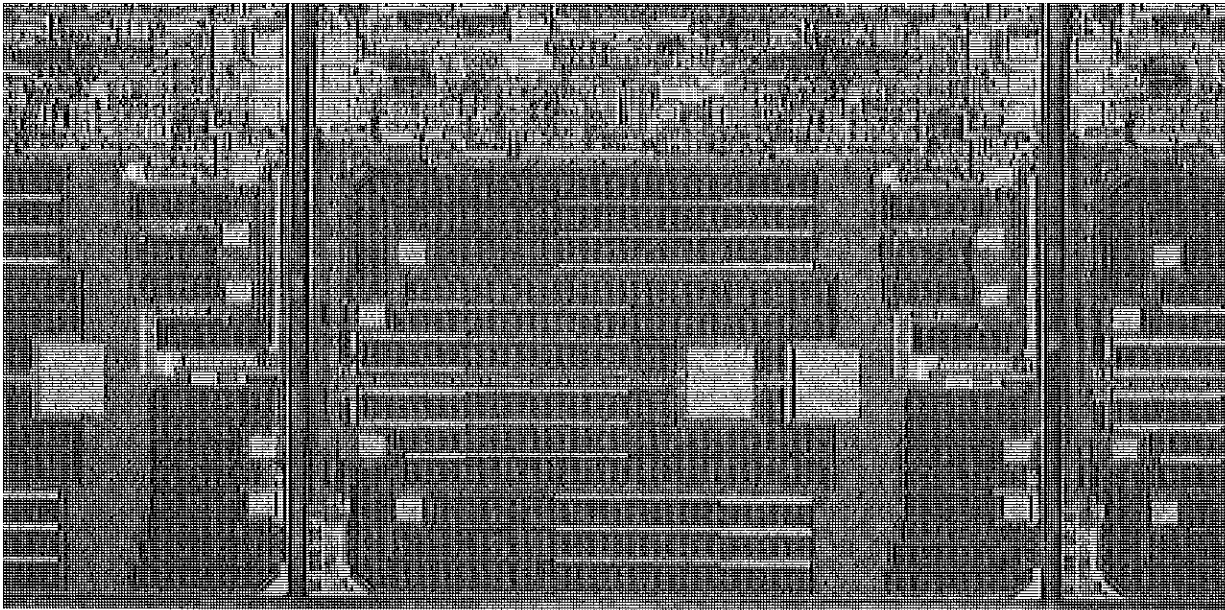
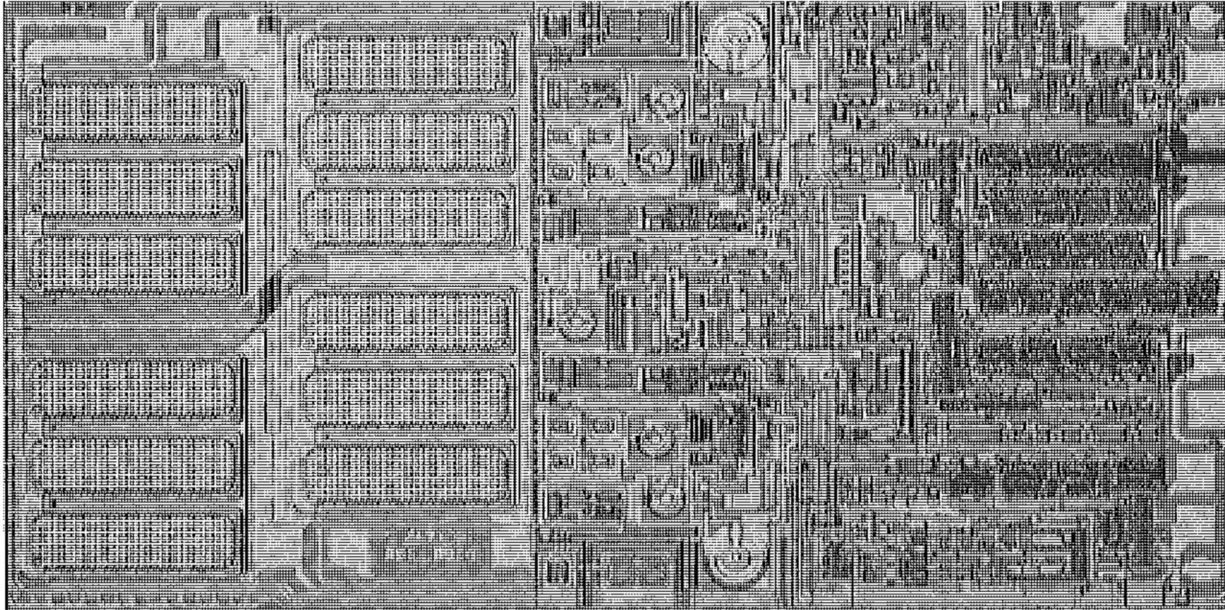


Figure 7: High Voltage IC for Electronic Lamp Ballast.

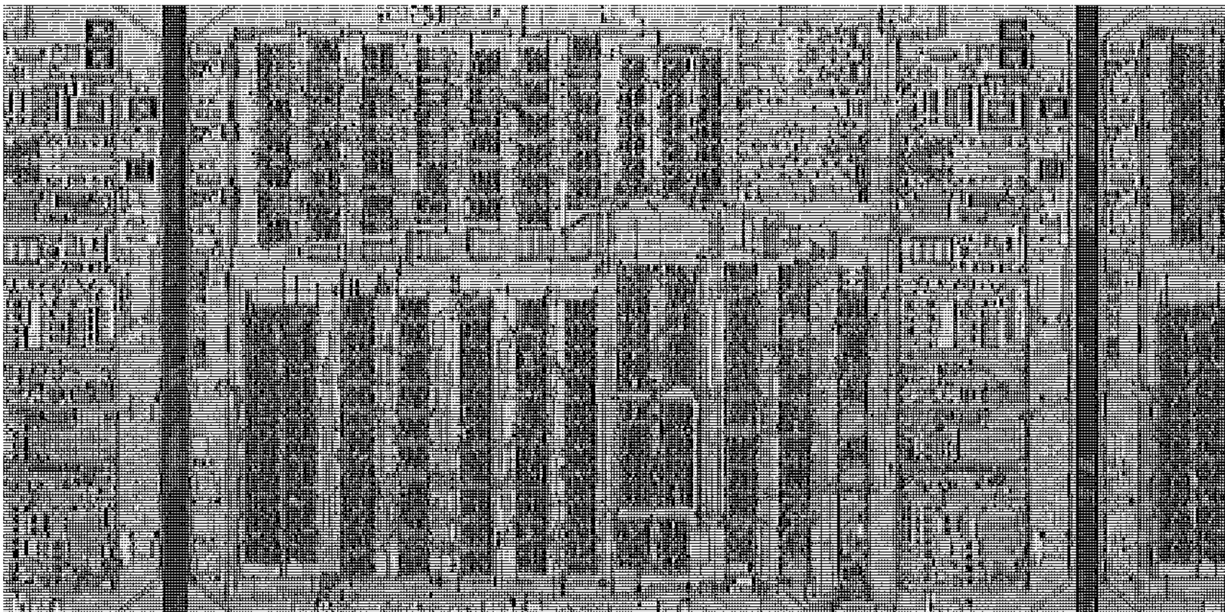


FAST DEVELOPMENT

The design of a BCD smart power IC, even a complex one, is surprisingly short. From the original idea to having a part working perfectly in the application takes typically six to ten months. These parts may not meet the original spec 100%, or SGS-THOMSON's yield standards, but they are good enough to use in production. Very complex ICs can be developed in roughly the same time because it is possible to divide the work between several designers. Unlike digital chips, in fact, a smart power IC is often designed by a single design engineer. This fast development is possible because such circuits almost always use just well known and predictable elements -- mainly library cells -- which are simply interconnected. And unlike linear power ICs, the DMOS power stages usually operate in switch-mode, which makes their behavior more predictable. The low power dissipation of power DMOS also helps because it minimizes unwanted thermal interactions.

In some cases the designer may also opt to use automatic layout techniques. This method is fast,

Figure 8: Example of Layout Generated Using Automatic Software Tools.



though it is not used where die size has to be reduced using manual layout. The circuit shown in figure 8 is an example of a BCD circuit laid out using automatic design tools.

Further time is saved by the application of 100% layout verification using CAD. This practically eliminates the risk of the first silicon not working because of a layout error.

PACKAGES

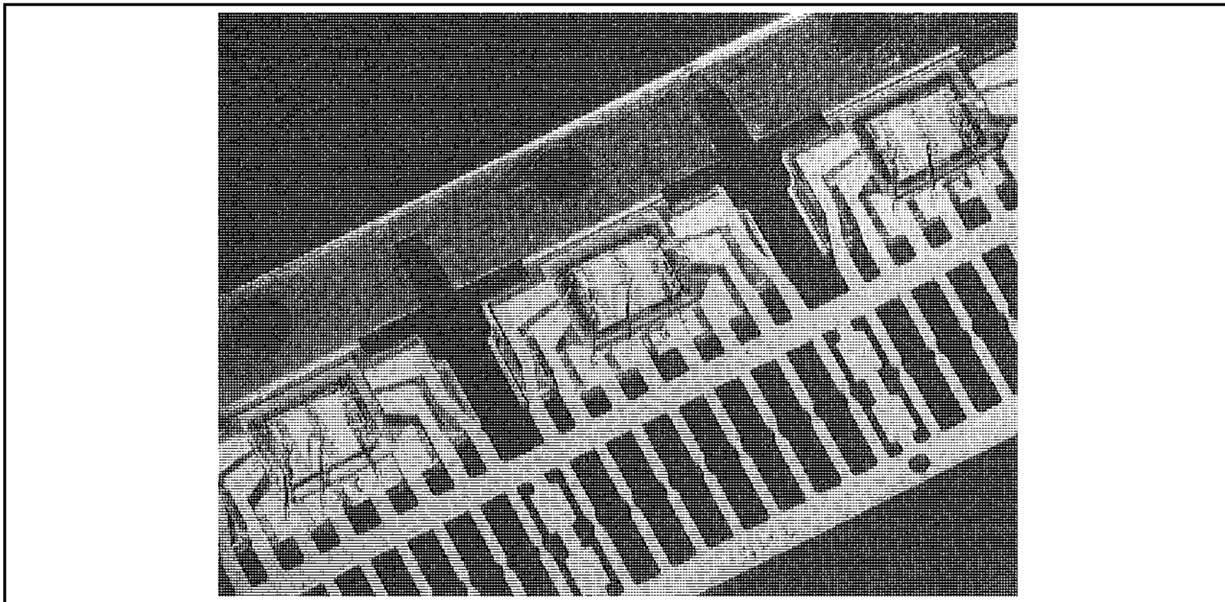
In power ICs, where dissipation is a fundamental limit, packaging very often determines both the performance and the cost of ICs. Fortunately for users of automatic assembly equipment in this area radically new packaging concepts are not expected in the near future. All of the ICs described here are, in fact, housed either in DIP, chip carrier or power packages like the Multiwatt 15-lead power tab package.

For high complexity types, where the pin count is generally high, plastic-leaded chip carrier PLCC packages are very popular. By modifying the lead frame, replacing all of the leads on one side by a triangular head spreader, it is possible to dissipate as much as 2.5W in a 44-lead PLCC. This is the package used for the chip in figure 1.

Where the highest output power is needed packages like the Multiwatt are used. To cope with the high currents involved in some circuits a mixed bonding technique has been developed for this package, using thick aluminum wires for the high current connections and thin gold wires for the others. An example of this is shown in figure 9, a 10A switching regulator IC. Thick aluminum could not be used for all connections because the large bonding pads required would waste too much silicon area; the use of multiple gold wires for power connections would compromise reliability.

BCD technology is often described as ”mixed”, primarily because it mixes bipolar, CMOS and digital. But it can also be described as mixed because it mixes analog and digital, because it mixes signal and power, because it mixes thick and thin metallization, and because of the mixed bonding technique.

Figure 9: An example of a power IC using mixed wire bonding.



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